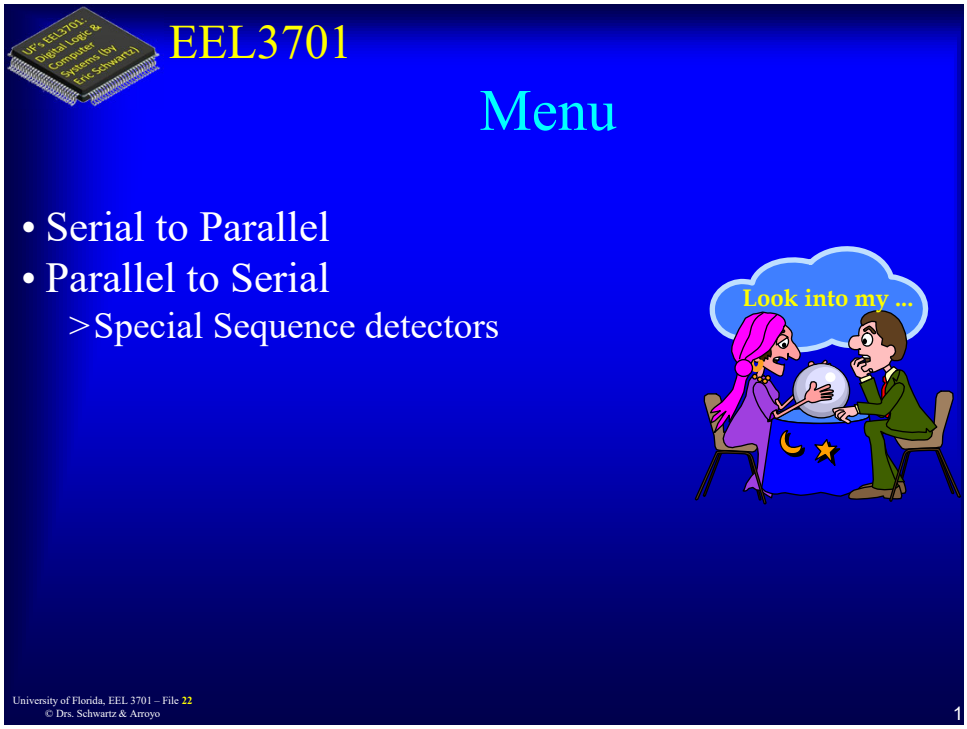
EEL3701
Menu
• Serial to Parallel
• Parallel to Serial
>Special Sequence detectors
Look into my ...
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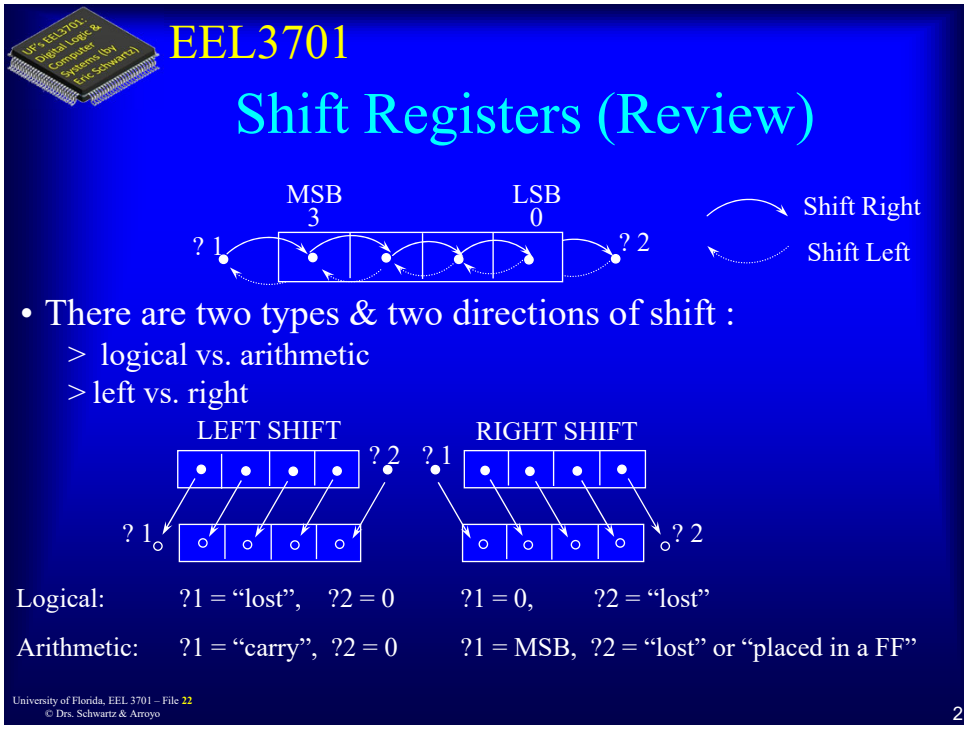
1

1


EEL3701
Shift Registers (Review)
MSB
3
LSB
0
? 1
? 2
Shift Right
Shift Left
• There are two types & two directions of shift :
> logical vs. arithmetic
> left vs. right
LEFT SHIFT
RIGHT SHIFT
? 2
? 1
? 1
? 2
Logical: ?1 = "lost", ?2 = 0 ?1 = 0, ?2 = "lost"
Arithmetic: ?1 = "carry", ?2 = 0 ?1 = MSB, ?2 = "lost" or "placed in a FF"
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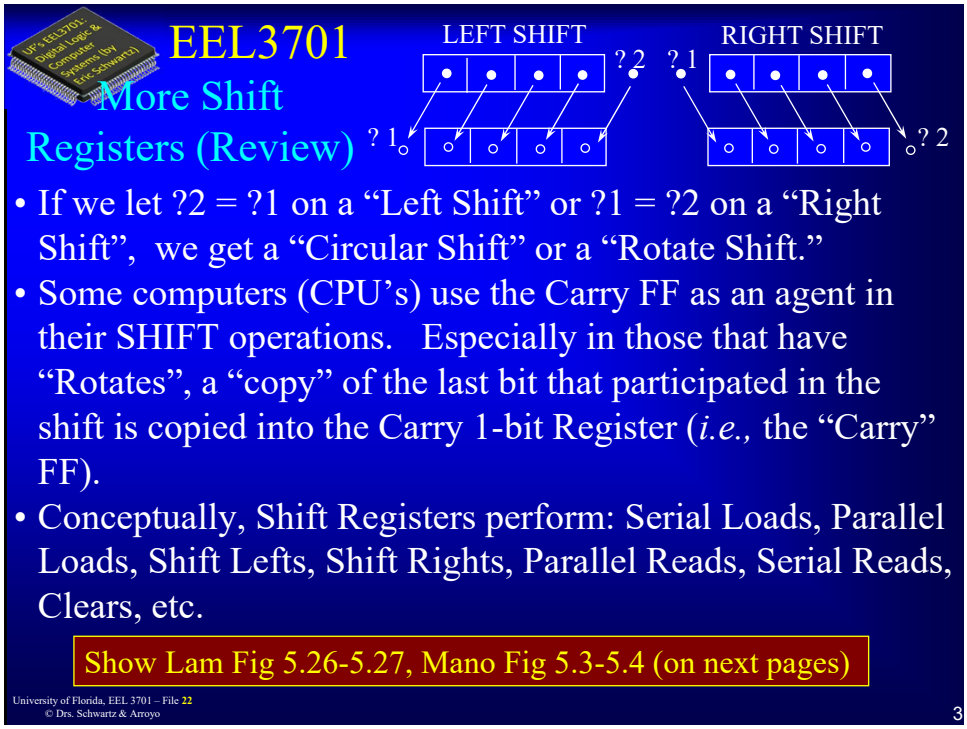
EEL3701
More Shift Registers (Review)
LEFT SHIFT
RIGHT SHIFT
?2
?1
?1
?2
• If we let ?2 = ?1 on a "Left Shift" or ?1 = ?2 on a "Right Shift", we get a "Circular Shift" or a "Rotate Shift."
• Some computers (CPU's) use the Carry FF as an agent in their SHIFT operations. Especially in those that have "Rotates", a "copy" of the last bit that participated in the shift is copied into the Carry 1-bit Register (*i.e.,* the "Carry" FF).
• Conceptually, Shift Registers perform: Serial Loads, Parallel Loads, Shift Lefts, Shift Rights, Parallel Reads, Serial Reads, Clears, etc.
Show Lam Fig 5.26-5.27, Mano Fig 5.3-5.4 (on next pages)
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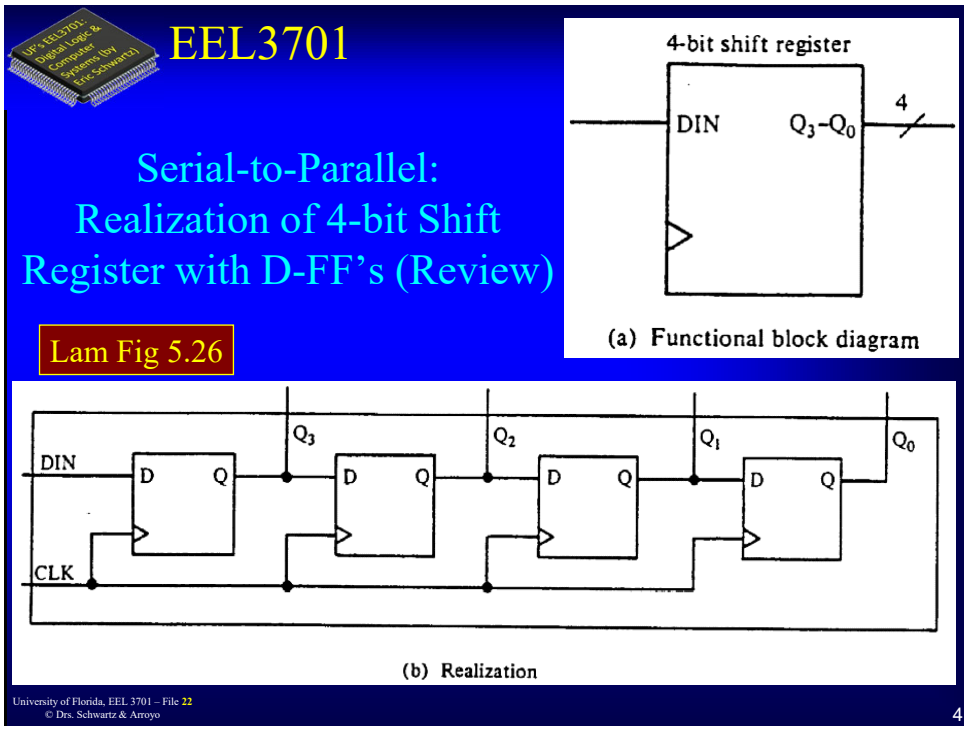
3

3


EEL3701
Serial-to-Parallel: Realization of 4-bit Shift Register with D-FF's (Review)
Lam Fig 5.26
4-bit shift register
DIN
Q_3-Q_0
4
(a) Functional block diagram
DIN
CLK
D
Q
Q_3
Q_2
Q_1
Q_0
(b) Realization
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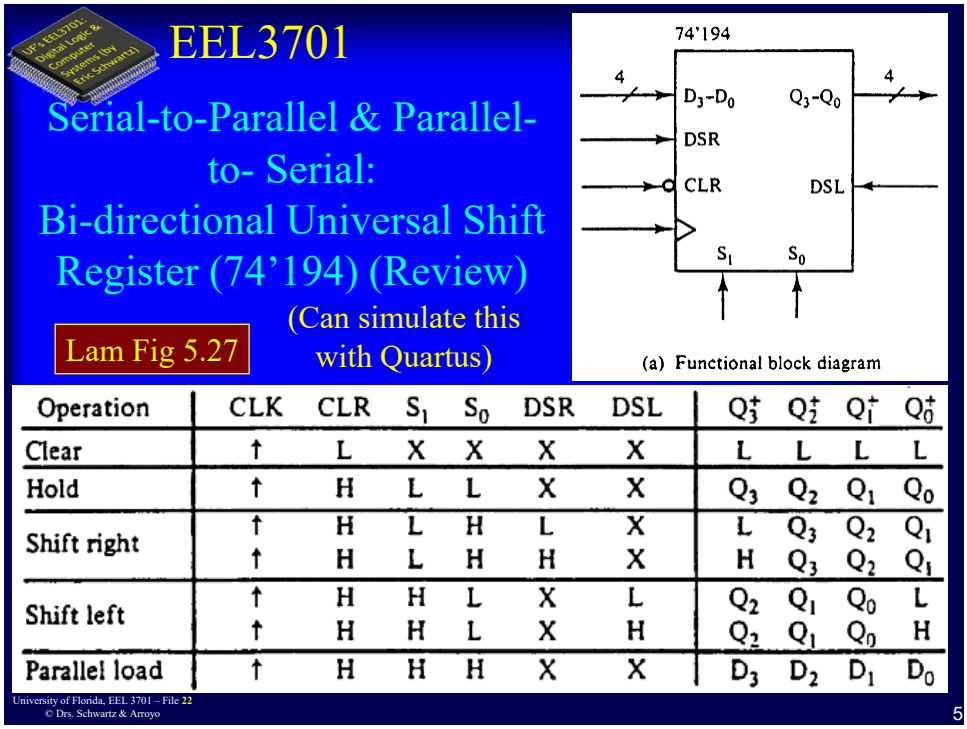
4

4


EEL3701
Serial-to-Parallel & Parallel-to- Serial: Bi-directional Universal Shift Register (74'194) (Review)
Lam Fig 5.27
(Can simulate this with Quartus)
74'194
4
D_3-D_0
Q_3-Q_0
4
DSR
CLR
DSL
S_1
S_0
(a) Functional block diagram
Operation | CLK | CLR | S_1 | S_0 | DSR | DSL | Q_3^+ | Q_2^+ | Q_1^+ | Q_0^+
Clear | ↑ | L | X | X | X | X | L | L | L | L
Hold | ↑ | H | L | L | X | X | Q_3 | Q_2 | Q_1 | Q_0
Shift right | ↑ | H | L | H | L | X | L | Q_3 | Q_2 | Q_1
↑ | H | L | H | H | X | H | Q_3 | Q_2 | Q_1
Shift left | ↑ | H | H | L | X | L | Q_2 | Q_1 | Q_0 | L
↑ | H | H | L | X | H | Q_2 | Q_1 | Q_0 | H
Parallel load | ↑ | H | H | H | X | X | D_3 | D_2 | D_1 | D_0
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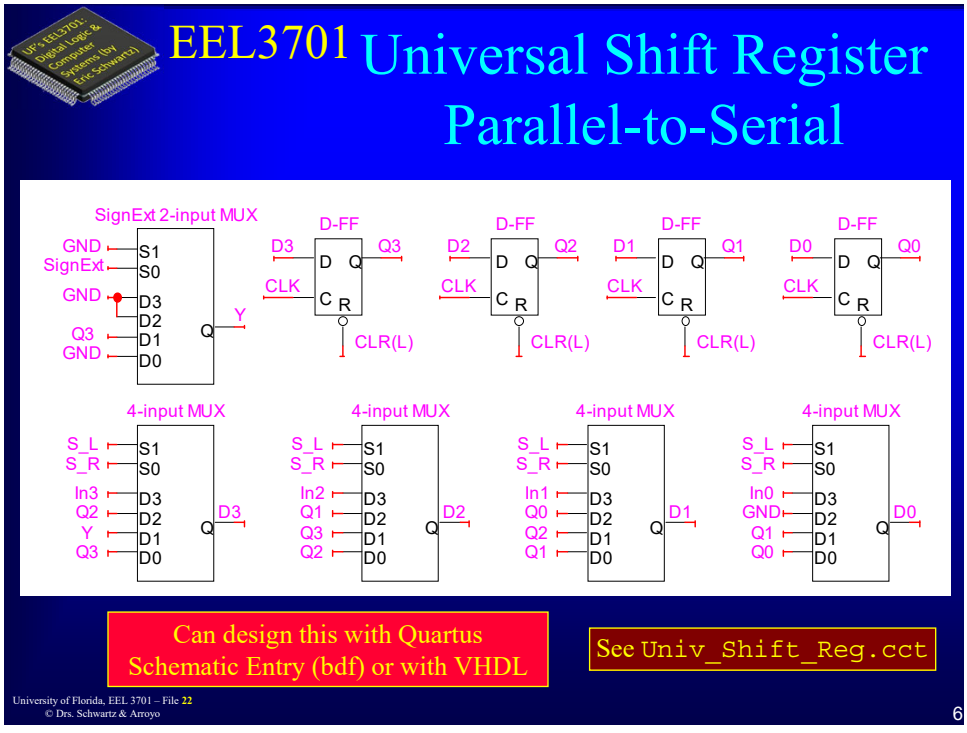
EEL3701 Universal Shift Register Parallel-to-Serial
SignExt 2-input MUX
GND
SignExt
GND
Q3
GND
S1
S0
D3
D2
D1
D0
Y
D-FF
D3
Q3
D2
Q2
D1
Q1
D0
Q0
CLK
CLR(L)
4-input MUX
S_L
S_R
In3
Q2
Y
Q3
In2
Q1
Q3
Q2
In1
Q0
Q2
Q1
In0
GND
Q1
Q0
D3
D2
D1
D0
Can design this with Quartus Schematic Entry (bdf) or with VHDL
See Univ_Shift_Reg.cct
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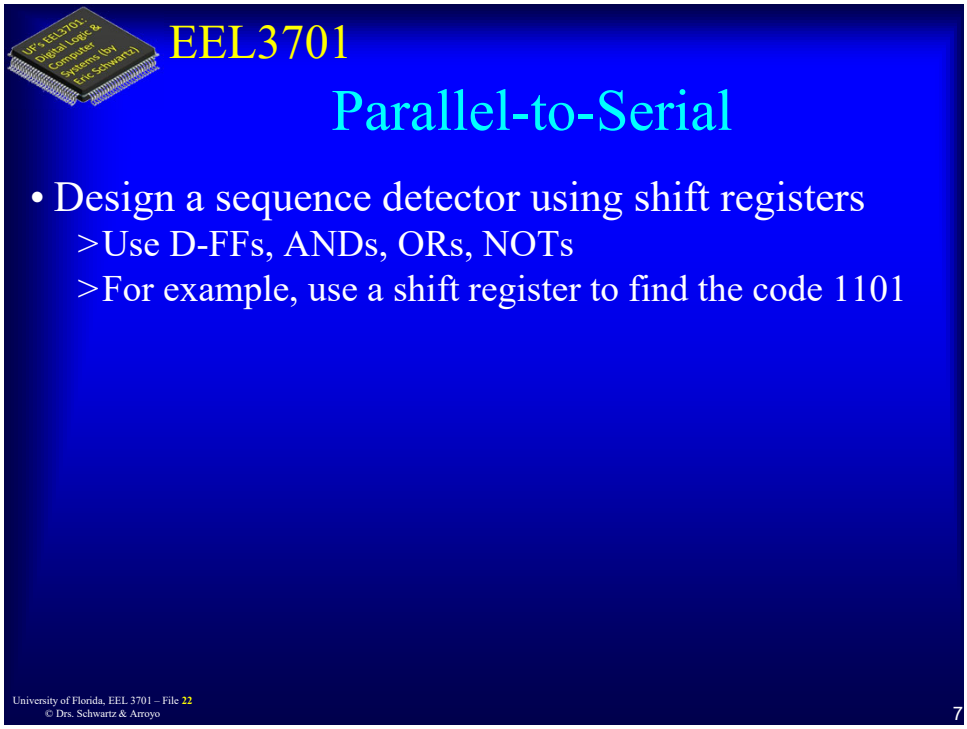
6


EEL3701
Parallel-to-Serial
• Design a sequence detector using shift registers
>Use D-FFs, ANDs, ORs, NOTs
>For example, use a shift register to find the code 1101
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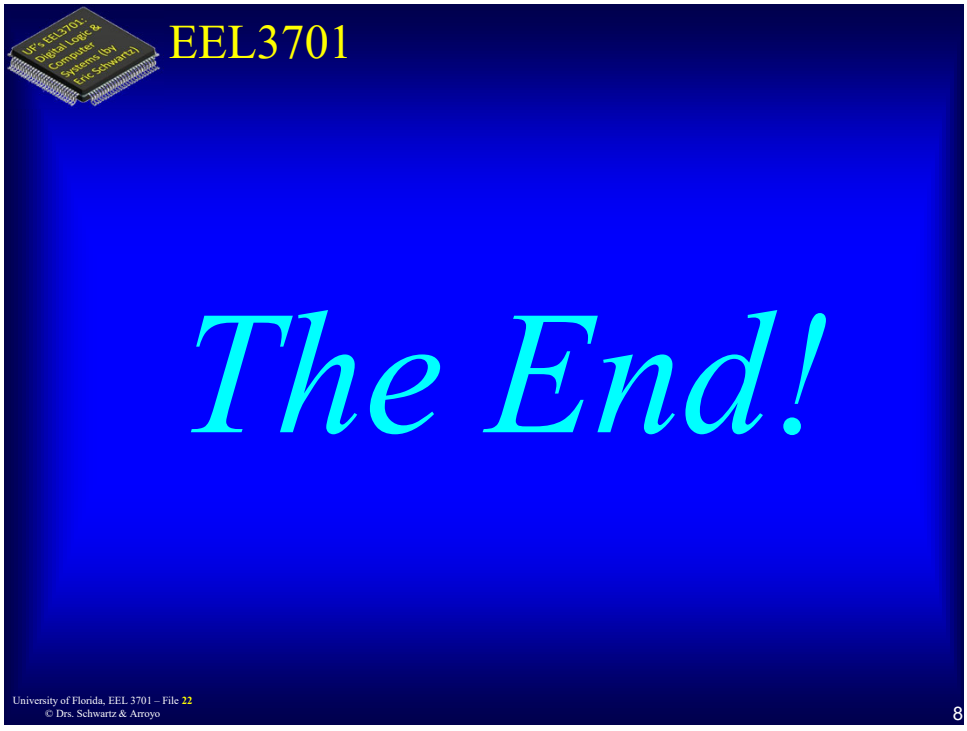
7

7


EEL3701
The End!
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